Subc1 Ist

1. (Amended) A nonvolatile memory comprising:

memory cell array including a plurality of memory cells being formed in a matrix, each of the memory cells including a memory thin film transistor and a switching thin film transistor,

wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating substrate;

a first insulating film;

a floating gate electrode;

a second insulating film;

a control gate electrode;

a wiring for connecting the control gate electrode with a first signal line,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating substrate;

a gate insulating film;

a gate electrode connected to a second signal line,

wherein the memory thin film transistor and the switching thin film transistor are integrally formed over the insulating substrate,

wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer of the switching thin film transistor,

B1 Concl'd

wherein the first semiconductor active layer of the memory thin film transistor is connected to a third signal line,

wherein the second semiconductor active layer of the switching thin film transistor is connected to a fourth signal line,

wherein the second signal line is formed between the semiconductor active layers and the first signal line,

wherein the first signal line and the second signal line are perpendicular to the third signal line and the fourth signal line,

wherein the floating gate electrode of the memory thin film transistor, the gate electrode of the switching thin film transistor, the first signal line and the second signal line are formed of a same layer, and

wherein the wiring of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer.

B2 Subc2

3. (Amended) A nonvolatile memory comprising:

a memory cell array including a plurality of memory cells being formed in a matrix, each of the memory cells including a memory thin film transistor and a switching thin film transistor,

wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating substrate;

a first insulating film;

a floating gate electrode;

B2 cont.

a second insulating film;

a control gate electrode;

a wiring for connecting the control gate electrode with a first signal line,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating substrate;

a gate insulating film;

a gate electrode connected to a second signal line,

wherein the memory thin film transistor and the switching thin film transistor are integrally formed over the insulating substrate,

wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is in a range of 1-100 nm while a second thickness of the second semiconductor active layer of the switching thin film transistor is in a range of 1-150 nm,

wherein the first semiconductor active layer of the memory thin film transistor is connected to a third signal line,

wherein the second semiconductor active layer of the switching thin film transistor is connected to a fourth signal line,

wherein the second signal line is formed between the semiconductor active layers and the first signal line,

wherein the first signal line and the second signal line are perpendicular to the third signal line and the fourth signal line,

B2 Concl'd

wherein the floating gate electrode of the memory thin film transistor, the gate electrode of the switching thin film transistor, the first signal line and the second signal line are formed of a same layer, and

wherein the wiring of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer.

Please add new claims 43-74 as follows.

Subc3 B3

43. (New) A nonvolatile memory comprising:

a memory cell array including a plurality of memory cells being formed in a matrix, each of the memory cells including a memory thin film transistor and a switching thin film transistor,

wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating substrate;

a first insulating film;

a floating gate electrode;

a second insulating film;

a control gate electrode,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating substrate;

a gate insulating film; and

a gate electrode connected to a second signal line,

133 Cont.

wherein the memory thin film transistor and the switching thin film transistor are integrally formed over the insulating substrate,

wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer of the switching thin film transistor,

wherein the control gate electrode of the memory thin film transistor is connected to the first signal line,

wherein the first semiconductor active layer of the memory thin film transistor is connected to a third signal line,

wherein the second semiconductor active layer of the switching thin film transistor is connected to a fourth signal line,

wherein the second signal line is formed between the semiconductor active layers and the first signal line,

wherein the first signal line and the second signal line are perpendicular to the third signal line and the fourth signal line,

wherein the floating gate electrode of the memory thin film transistor, the gate electrode of the switching thin film transistor, the first signal line and the second signal line are formed of a same layer, and

wherein control gate electrode of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer.

B3 cont

44. (New) A memory according to claim 43, wherein each of the first and second thicknesses is in a range of 1-150 nm.

Sub C4

45. (New) A nonvolatile memory comprising:

a memory cell array including a plurality of memory cells being formed in a matrix, each of the memory cells including a memory thin film transistor and a switching thin film transistor,

wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating substrate;

a first insulating film;

a floating gate electrode;

a second insulating film;

a control gate electrode,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating substrate;

a gate insulating film; and

a gate electrode connected to a second signal line,

wherein the memory thin film transistor and the switching thin film transistor are integrally formed over the insulating substrate,

wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island,

B3 cont.

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is in a range of 1-100 nm while a second thickness of the second semiconductor active layer of the switching thin film transistor is in a range of 1-150 nm,

wherein the control gate electrode of the memory thin film transistor is connected to the first signal line,

wherein the first semiconductor active layer of the memory thin film transistor is connected to a third signal line,

wherein the second semiconductor active layer of the switching thin film transistor is connected to a fourth signal line,

wherein the second signal line is formed between the semiconductor active layers and the first signal line,

wherein the first signal line and the second signal line are perpendicular to the third signal line and the fourth signal line,

wherein the floating gate electrode of the memory thin film transistor, the gate electrode of the switching thin film transistor, the first signal line and the second signal line are formed of a same layer, and

wherein the control gate electrode of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer.

46. (New) A memory according to claim 43, wherein the first thickness in a range of 1-50 nm while the second thickness is in a range of 10-100 nm.

47. (New) A memory according to claim 43, wherein the first thickness is in a range of 10-40 nm.

B3 cont.

48. (New) A memory according to claim 43, wherein each of the memory thin film transistor and the switching thin film transistor is a p-channel thin film transistor.

49. (New) A memory according to claim 43, further comprising a driver circuit for driving the plurality of memory cells, wherein the memory cell array and the driver circuit are integrally formed over the insulating substrate.

50. (New) A semiconductor device including the nonvolatile memory of claim 43, said semiconductor device further comprising:

a pixel portion;

a driver circuit for driving the pixel portion,

wherein the pixel portion, the driver portion and the nonvolatile memory are integrally formed over the insulating substrate.

51. (New) A semiconductor device according to claim 50, wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

52. (New) A semiconductor device according to claim 50, wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

B3 cont.

53. (New) A memory according to claim 45, wherein the first thickness in a range of 1-50 nm while the second thickness is in a range of 10-100 nm.

54. (New) A memory according to claim 45, wherein the first thickness is in a range of 10-40 nm.

55. (New) A memory according to claim 45, wherein each of the memory thin film transistor and the switching thin film transistor is a p-channel thin film transistor.

56. (New) A memory according to claim 45, further comprising a driver circuit for driving the plurality of memory cells, wherein the memory cell array and the driver circuit are integrally formed over the insulating substrate.

57. (New) A semiconductor device including the nonvolatile memory of claim 45, said semiconductor device further comprising:

a pixel portion;

a driver circuit for driving the pixel portion,

wherein the pixel portion, the driver portion and the nonvolatile memory are integrally formed over the insulating substrate.

B3 cont.

58. (New) A semiconductor device according to claim 57, wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

59. (New) A semiconductor device according to claim 57, wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

Sub C5

60. (New) A semiconductor device comprising:

a memory cell array comprising a plurality of memory cells formed over a substrate in a matrix, each of the memory cells comprising:

a memory thin film transistor comprising a first semiconductor active layer formed on an insulating surface, a floating gate electrode and a first control gate electrode; and

a switching thin film transistor electrically connected to the memory thin film transistor, said switching thin film transistor comprising a second semiconductor active layer formed on the insulating surface and a second gate electrode,

B3 cont.

a first signal line and a second signal line extending in parallel in a first direction over the substrate, said first signal line being electrically connected to the control gate electrode of the memory thin film transistor and said second signal line being electrically connected to the second gate electrode of the switching thin film transistor;

an interlayer insulating film formed over the first signal line and the second signal line;

a third signal line and a fourth signal line formed over the interlayer insulating film and extending in parallel in a second direction orthogonal to the first direction said third signal line being electrically connected to one of source and drain regions of the memory thin film transistor and said fourth signal line being electrically connected to one of source and drain regions of the switching thin film transistor; and

a conductive film formed over the interlayer insulating film, said conductive film electrically connecting said first signal line and said control gate electrode of the memory thin film transistor,

wherein the first semiconductor active layer and the second semiconductor active layer of one of the memory cells are formed in a common semiconductor island,

wherein the floating gate electrode of the memory thin film transistor, the second gate electrode of the switching thin film transistor, and the first and second signal lines are formed of a same layer,

wherein the third and fourth signal lines and said conductive film are formed of a same layer, and

wherein said conductive film extends across the second signal line.

61. (New) A semiconductor device according to claim 60, wherein said first semiconductor active layer has smaller thickness than the thickness of said second semiconductor active layer.

B3 Cont.

62. (New) A semiconductor device according to claim 60, wherein each of the first and second thicknesses is in a range of 1-150 nm.

63. (New) A semiconductor device according to claim 60, wherein the first thickness is in a range of 1-50 nm while the second thickness is in a range of 10-100 nm.

64. (New) A semiconductor device according to claim 60, wherein the first thickness is in a range of 10-40 nm.

65. (New) A device according to claim 60, wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

Sub C4

66. (New) A semiconductor device comprising:

a display portion comprising a plurality of pixel thin film transistors over a substrate;

B3 Cont.

a memory cell array comprising a plurality of memory cells formed over a substrate in a matrix, each of the memory cells comprising:

a memory thin film transistor comprising a first semiconductor active layer formed on an insulating surface, a floating gate electrode and a first control gate electrode; and

a switching thin film transistor electrically connected to the memory thin film transistor, said switching thin film transistor comprising a second semiconductor active layer formed on the insulating surface and a second gate electrode;

a first signal line and a second signal line extending in parallel in a first direction over the substrate, said first signal line being electrically connected to the control gate electrode of the memory thin film transistor and said second signal line being electrically connected to the second gate electrode of the switching thin film transistor;

an interlayer insulating film formed over the first signal line and the second signal line;

a third signal line and a fourth signal line formed over the interlayer insulating film and extending in parallel in a second direction orthogonal to the first direction, said third signal line being electrically connected to one of source and drain regions of the memory thin film transistor and said fourth signal line being electrically connected to one of source and drain regions of the switching thin film transistor; and

a conductive film formed over the interlayer insulating film and electrically connecting said first signal line and said control gate electrode of the memory thin film transistor,

133 Cont.

wherein the first semiconductor active layer and the second semiconductor active layer of one of the memory cells are formed in a common semiconductor island,

wherein the floating gate electrode of the memory thin film transistor, the second gate electrode of the switching thin film transistor, and the first and second signal lines are formed of a same layer,

wherein the third and fourth signal lines and said conductive film are formed of a same layer, and

wherein said conductive film extends across the second signal line.

67. (New) A semiconductor device according to claim 66, wherein said first semiconductor active layer has smaller thickness than the thickness of said second semiconductor active layer.

68. (New) A semiconductor device to according to claim 66, wherein each of the first and second thickness values is in a range of 1-150 nm.

69. (New) A semiconductor device according to claim 66, wherein the first thickness is in a range of 1-50 nm while the second thickness is in a range of 10-100 nm.

70. (New) A semiconductor device according to claim 66, wherein the first thickness is in a range of 10-40 nm.

71. (New) A semiconductor device according to claim 66, further comprising an active matrix circuit of a display device over said substrate.

B3 Cont.

72. (New) A semiconductor device according to claim 66, wherein said pixel portion comprises an electroluminescence layer.

73. (New) A semiconductor device according to claim 66, wherein said pixel portion comprises a liquid crystal.

74. (New) A semiconductor device according to claim 66, wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.